UNIVERSITY OF CALIFORNIA
Department of Electrical Engineering and Computer Sciences
EE130 Fall 2004

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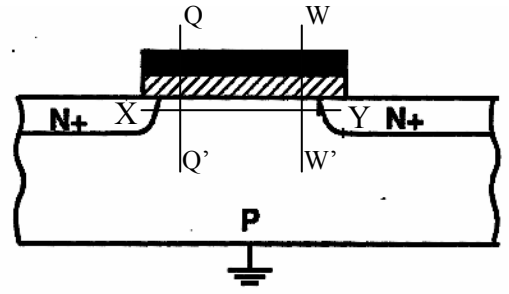
Test 4

1) You are given two NMOSFETs with identical doping, gate oxide thickness, and junction depth.
   - MOSFET "A" has a punchthrough voltage of 10V
   - MOSFET "B" has a punchthrough voltage of 20V

   a) Which device has a shorter L? Give reasons for your answer.

2 pts

   b) Suppose MOSFET "A" has a V_T of 0.5V. Sketch a band diagram for MOSFET "A" along slice Q-Q' (shown below) for V_{DS} = 1.0V and V_{GS} = 1.5V. Also sketch a band diagram for the same device along the W-W' slice. Make sure you clearly identify any differences between the two slices.



5 pts

c) Which device ("A" or "B") would you expect to have a higher small-signal output resistance? Why?

2 pts

d) Suppose I took MOSFET "A", and increase the channel doping. Assume I change the gate workfunction so that the threshold voltage stays unchanged.

i) What would be the impact on the output resistance? Give reasons.

2 pts

i) When I changed the gate workfunction – should I have increased it or decreased it to keep the V_T constant.

1 pt

e) Suppose I were to operate MOSFET "A" at $V_{DS} = 0.5V$ and $V_{GS} = 0.4V$ (As in part (b), assume the V_T is 0.5V). What phenomenon is responsible for current to flow between the source and the drain? Explain the mechanism behind this.

2 pts

f) Assume MOSFET "A" has a series resistance that is approximately 25% of the large-signal channel resistance (I_{Dsat}/V_{DS}). Draw a band diagram for MOSFET along slice X-Y for MOSFET A, assuming $V_T = 0.5V$, $V_G = 1V$, and $V_D = 1V$. Make sure you include the source/drain regions in your band diagram.

5 pts

2) In recent years, for various reasons, I_{Dsat} in MOSFETs is no longer increasing with decreasing channel length; rather, it has become almost constant from generation to generation for devices with the same channel width, despite the fact that L is decreasing steadily. Given this fact, why do we continue to scale L? Justify your answer in terms of both speed and power consumption metrics. (Hint: consider the impact of constant field scaling on capacitance)

3 pts

3) One of the important parameters that must be scaled is t_{ox}. Discuss any problems that might exist with the continued scaling of t_{ox} in terms of the following:

i) The use of a polysilicon gate

1 pt

ii) The effect of the quantum mechanical inversion charge centroid

1 pt

iii) The effect of tunneling current through the gate oxide as the gate thickness is reduced.

1 pt